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09/575,560	05/21/2000	Paul Ferguson	A0312/7409/MXS	1265

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EXAMINER

PHAN, TRONG Q

ART UNIT

PAPER NUMBER

2818

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/575,560

Applicant(s)

FERGUSON ET AL.

Examiner

TRONG PHAN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on May 13, 2002
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above, claim(s) 10-15, 25, 26, and 30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9, 16-24, 27-29, and 31-40 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show: the mixer 72[✓] (line 5, page 10), the inverter 174[✓] (line 17, page 12); the (reference voltage Vref (line 26, page 13), the reference voltages V2, V4, V6, V8 are connected to ground (line 26, page 13), the switches 148, 149 and 150[✓] (line 18, page 20), (the non overlapping four phase clock (line 9, page 27), the output of the input op amp (line 16, page 27); and the latch stage 804 (line 17, page 33) as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-9, 16-24, 27-29 and 31-40 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

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Claims 1-9, 16-24, 27-29 and 31-40 are not clearly understood because of the following reasons:

1) the specification does not describe the following features: the mixer circuit in Fig. 2; the QDAC1 to QDACN and the charge sharing network in Fig. 4; the elements 176 and $P1 + P2$ in Fig. 5; Fig. 6; the master clock and signal P4 in Fig. 9; the switch connected between element 164 and S19 in Fig. 10; all elements in Figs. 28A-B; all the switches, capacitors and elements from SCF, selectable gain, External CAP and Voltage output in Fig. 30; and elements $P1 + \text{bit1}.P2$, $P1 + \text{bit2}.P2$, $P1 + \text{bit3}.P2$ and $P1 + \text{bit4}.P2$ in Fig. 31; *Phase signal P2 (line 31, page 29)* ?

2) all equations in Figs. 7A-C, 8A-D and 12A-C, 14A-C, 19A-C, 33A-C and 34A-C are not clearly understood since the V_{ref} and $Q(C1)$, $Q(C2)$, $Q(C3)$ and $Q(C4)$ are not described in the specification; the switching ON/OFF operation of all the switches in each of Figs. 11A-D, 15, 16A-E, 17-18, 19A-C, 20-22, 25, 27 and 30 is not understood since no switching control signal is shown in the drawings and is described in the specification; the connection of each of elements 202, 204, 206, 208, S49 and S50 in Fig. 15 is not completely described in the specification; the connection of each of elements S43 and S48 in Fig. 16A-E is not completely described in the specification; it is not clear how terminals 312 and 314 in Figs. 16B-E are interconnected with each other; elements NC, NAND gates, inverters, switches, capacitors and terminals in Figs. 17, 21-22, 25 are not

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described as well as numbered; the four arrows on the right side of scrambler 400 are not described as well as numbered; all capacitors in Fig. 27 are not described as well as numbered;

in Fig. 24

3) the feature "an analog signal that is indicative of the multi-bit input signal received by the switched capacitor DAC using less than all of the redistributed charge" as recited in last three lines of claim 29 is not described in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-9 and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fling et al., 4,591,832, in view of Mehta et al., 4,205,203, Lee et al., 6,130,633, and Dingwall et al., 5,332,997.

Fling et al., 4,591,832, discloses in Fig. 1 a system comprising: signal preconditioner 12 for alternately providing digital samples of PCM binary samples in the luminance signal processing channel of a digital TV receiver (see lines 3436, column 2) to the common input of both DACs 16 and 18 connected in

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parallel (see lines 42-48, column 2); therefore, the first output analog signal 20 from the first DAC 16 is seen to be indicative of a sum of values of the input digital samples of PCM binary samples from signal preconditioner 12; and , alternately, the second output analog signal 22 from the second DAC 18 is seen to be indicative of a sum of values of the input digital samples of PCM binary samples from signal preconditioner 12 thereof; summing circuit 24 for producing the system common output signal at terminal 25.

What is not shown in Fling et al., 4,591,832, is the multi-bit digital signal as recited in claims 1-4 and 13-52.

Mehta et al., 4,205,203, discloses the teaching that digital samples of PCM binary samples are in the form of multi-bit digital signal (see the Summary of The Invention, lines 64-68, column 1 and lines 1-68, column 2).

In view of the above teaching of Mehta et al., 4,205,203, the input digital samples of PCM binary samples in the luminance signal processing channel of a digital TV receiver provided to the common input of both DACs 16 and 18 in Fig. 1 of Fling et al., 4,591,832, would have been obviously in the form of multi-bit digital signal as recited in claims 1-4 and 13-52.

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What is not shown in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203, is the signal conditioning stage comprising a switched capacitor filter as recited in claims 1-4 and 13-52.

Lee et al., 6,130,633, discloses in Fig. 2A Prior Art the teaching of using switched capacitor filter 210 to be connected to the output of DAC 200.

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the switched capacitor filter 210 in Fig. 2A of Lee et al., 6,130,633, for connecting to the system common output terminal 25 in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203, for the purpose of performing of lowpass filtering for removal of quantization noise in the system common output analog signal at common output terminal 25 in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203 (see lines 5-7, column 4 of Lee et al., 6,130,633).

Lee et al., 6,130,633, discloses in Fig. 2A Prior Art the teaching of using switched capacitor filter 210 to be connected to the output of DAC 200.

It would have been obvious under 35 U.S.C. 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the switched capacitor filter 210 in Fig. 2A of Lee et al., 6,130,633, for connecting to the system common output terminal 25 in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203, for the purpose of performing of lowpass filtering for

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removal of quantization noise in the system common output analog signal at common output terminal 25 in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203 (see lines 5-7, column 4 of Lee et al., 6,130,633).

What is not shown in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203, and Lee et al., 6,130,633, is the plurality of capacitors connecting to one another to share charge with one another as recited in claim 6.

Dingwall et al., 5,332,997, discloses in Fig. 2 a DAC comprising a plurality of capacitors C0-C5 sharing charge with one another.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the DAC in Figs. 2 of Dingwall et al., 5,332,997, for the DACs 16 and 18 in Fig. 1 of Fling et al., 4,591,832, which is modified by Mehta et al., 4,205,203, and Lee et al., 6,130,633, for the purpose of loading data at a high speed (see lines 29-35, column 3 of Dingwall et al., 5,332,997).

6. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita, 5,890,432, in view of Dingwall et al., 5,332,997.

Yamashita, 5,890,432, discloses in Fig. 4 a handset for a mobile communication system including:

input stage 105 receiving multi-bit digital signals TxD1 to TxDQ;

digital to analog converter D/A 307.

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What is not shown in Yamashita, 5,890,432, is the switched capacitor network having a plurality of DACs as recited in claim 27.

Dingwall et al., 5,332,997, discloses in Fig. 6 a system having a switched capacitor D/A converter network comprising a plurality of DACs 11 which each has a detailed structure, as shown in Fig. 2, comprising a plurality of capacitors C0-C5 sharing charge with one another.

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the invention was made to utilize the DAC in Figs. 2 and 6 of Dingwall et al., 5,332,997, for the digital to analog converter D/A 307 in Fig. 4 of Yamashita, 5,890,432, for the purpose of loading data at a high speed (see lines 29-35, column 3 of Dingwall et al., 5,332,997).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371^o of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application

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as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

8. Claims 17-24, 28-33 and 38-40 are, insofar as definite, rejected under 35 U.S.C. 102(e) as being anticipated by Watson et al., 6,154,162.

Watson et al., 6,154,162, discloses in Fig. 4 a digital signal processing system comprising:

scrambler 42;

switched capacitor DAC 32 including a plurality of capacitors 70, 72 and 74 sharing charge with each other.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164

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USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321[©] may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1-9 and 34-37 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-17 of copending Application No. 09/575,561. Although the conflicting claims are not identical, they are not patentably distinct from each other because the two analog signals as recited in claims 1-9 and 34-37 of the present application are obviously read on the two analog signals as recited in claims 1-17 of copending Application No. 09/575,561.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

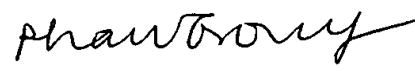
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Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **TRONG PHAN** whose telephone number is (703) 308-4870 and email address is trong.phan@uspto.gov


TRONG PHAN
PRIMARY EXAMINER

June 18, 2002